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10/520,328	01/04/2005	David A. Fish	GB02 0108 US	5114

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EXAMINER	
CARTER III, ROBERT E	
ART UNIT	**PAPER NUMBER**
2609	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/520,328	FISH ET AL.	
	Examiner	Art Unit	
	Robert E. Carter	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/04/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5 and 7-12* is/are rejected.

7)☒ Claim(s) *3,6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 5, 7-10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishitani et al. (US Patent # 5,764,212) in view of Edwards (US Patent # 5,448,258).

As for claim 1 and 12,

Nishitani et al. teaches:

A display component, and method for decoding and

displaying data coded using a transform having basis functions; comprising: a plurality of pixels (Fig. 2) arranged as a block (Fig. 55, Walsh 1, Col 32, lines 50-65);

A first element (Fig. 42, #126) providing a unit positive contribution to the summing element;

A first switch (Fig. 40, #135[switch connected to voltage line 126]) connecting the first element to the summing element;

A second element (Fig. 42, #127) providing a unit negative contribution to the summing element; a second switch (Fig. 40, #135[switch connected to voltage line 127]) connecting the second element to the summing element;

control circuitry (Fig. 40, #122) connected to the first and second switches for switching the first and second switches in accordance with basis function values;

the display component further comprising a modulator (Fig. 37, #39, 118, 120) for modulating all the first and second elements of the pixels of a block in common in accordance with input data, so that the summing element accumulates decoded input data for display in accordance with the input data and the basis function values.

Nishitani et al. does not teach:

Each pixel including:

A summing element

A first element

A first switch

A second element

A second switch

And control circuitry

Edwards teaches:

A display component (Fig. 1), and method for decoding and displaying coded data comprising a plurality of pixels (Fig. 1, #12), each pixel including a summing element (Fig. 3, #C1).

The examiner would also point out that while the summing element is absent from the drawings of Nishitani et al., The overlap of any two electrodes such as X0 and Y0 in figure 2 of Nishitani et al. creates a capacitive element capable of storing (and hence summing) any charges applied to the electrodes.

Edwards further teaches that decoders may be located in the column driver (Col. 1, line 31 – Col. 2, line 5), or in the pixel elements (Col. 2, lines 31-58) and that locating them in the pixel elements simplifies circuit design, TFT substrate fabrication, and increases performance.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to add the summing element in Edwards to the output of the display component in Nishitani et al., and further to move the decoder in Nishitani et al. from the

column driver into the pixel elements to simplifies circuit design, TFT substrate fabrication, and increases performance, as taught in Edwards.

As for claim 5,

Nishitani et al. in view of Edwards teaches all the limitations of claim 1, and further teaches:

A display component comprising:

A plurality of the blocks (Fig. 55, Walsh1 - Walsh60) are arranged in rows (Fig. 55, 1st division – 60th division) and columns (Fig. 55, [Y1-Y4] – [Y237-Y240]), each row of blocks having a block select line (Fig. 64, #180) for selecting that row of blocks; wherein the pixel elements of each row of blocks only operate to decode data when selected by the block select line.

As for claim 7,

Nishitani et al. in view of Edwards teaches all the limitations of claim 1, and further teaches:

A display component wherein:

The control circuitry of each pixel has row (Fig. 40, #115) and column (Fig. 40, #121) basis function inputs; further comprising:

row basis function lines (Fig. 65, #144) connected to the row basis function input of

each pixel element of a row of pixel elements of a block; and

column basis function lines (Fig. 60, four unlabeled lines at bottom of drawing) connected to the column basis function input of each pixel element of a column of pixel elements of a block; and

wherein the at least one basis function generator (Fig. 56, #143) generates basis functions for each row and column and outputs the basis functions on respective outputs connected to respective row and column basis function lines.

As for claim 8,

Nishitani et al. in view of Edwards teaches all the limitations of claim 7, and further teaches:

A display component wherein the control circuitry has an XOR gate (Fig. 40, #122) having the XOR gate inputs connected to the row and column basis function inputs and the XOR gate output connected to one of the first and second switches directly and the other of the first and second switches through an inverter (Fig. 40, #122).

As for claim 9,

Nishitani et al. in view of Edwards teaches all the limitations of claim 1, and further teaches:

A display component wherein the basis functions are Walsh basis functions (Fig. 55, Col 33, lines 15-17).

As for claim 10,

Nishitani et al. in view of Edwards teaches all the limitations of claim 1, and further teaches:

A liquid crystal display, comprising an active plate, a passive plate, and liquid crystal between the active and passive plates (Edwards Col. 5, line 45 – Col. 6, line 9).

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nishitani et al. (US Patent # 5,764,212) in view of Edwards (US Patent # 5,448,258) and further in view of Shanks et al. (US Patent # 5,747,928)

As for claim 11,

Nishitani et al. in view of Edwards teaches all the limitations of claim 1, however, they do not teach the limitations of claim 11.

Shanks et al. teaches:

A display component wherein each pixel element further includes a polymer light emitting diode (Abstract lines 1-4) for emitting light in accordance with the decoded input data on the summing element.

Shanks et al. further teaches that this display is better than prior displays because it can be flexed without damage to the display (Col. 8, lines 9-19).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the display component in Nishitani et al. in view of Edwards by adding the polymer light emitting diodes in Shanks et al. to emit light in accordance with the decoded input data on the summing element while allowing the display to be flexed without damage.

5. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishitani et al. (US Patent # 5,764,212) in view of Edwards (US Patent # 5,448,258) and further in view of Hunter et al. (US Patent # 6,577,302) and Abe et al. (US Patent # 6,839,054).

As for claim 2,

Nishitani et al. in view of Edwards teaches all the limitations of claim 1, however, they do not teach the limitations of claim 2.

Hunter et al. teaches:

A capacitive summing element (Fig. 5, Ci), the voltage on the capacitance determining the pixel output;

A first element (Fig. 5, #10) providing a unit positive contribution to the summing element, the first element consisting of an N-channel TFT functioning as a modulated current source for charging the capacitance

A second switch (Fig. 5, #S1) connected to the summing element;

Hunter et al. does not teach:

A second element providing a unit negative contribution to the summing element, the second element consisting of a modulated current sink for discharging the capacitance.

Abe et al. teaches:

A driving circuit for a panel display comprising a positive supply (Fig. 1, Vdd) supplying a positive current source (Fig. 1, I1) and a negative supply ((Fig. 1, Vss) supplying a negative current source (Fig. 1, Vss) the output of the two current sources connected to a two way switch such that it either sources or sinks current to the display pixel element.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the pixel driver in Hunter et al. by adding a negative supply and a second element comprising a P-channel TFT functioning as a negative current source, as disclosed in Abe et al., to enable AC positive/negative driving of the pixel, a

driving method with the well known benefit of prolonging display life (Fujita, US Patent # 3,781,864 Col. 1, lines 9-17).

It further would have been obvious to that person of ordinary skill to modify the first and second elements in Nishitani et al. in view of Edwards by replacing them with the first and second elements in Hunter et al. in view of Abe et al. and connecting their control terminals (Fig. 5, Vref) through common data lines to the modulator in Nishitani et al. in view of Edwards, to allow the driver in Nishitani et al. in view of Edwards to drive current driven display pixels.

Allowable Subject Matter

6. Claims 3 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Tsuchi et al. (US Patent # 6,909,414) discloses a liquid crystal display driver.

Fukuo (US Patent # 6,496,175) discloses an output circuit for a liquid crystal display driver.

Nakao (US Patent # 6,437,716) discloses a grey scale liquid crystal display driver.

Walsh (US Patent # 6,351,327) discloses a current sensing liquid crystal display driver.

Shigeta (US Patent # 6,091,385) discloses a flat panel display driver.

Sato et al. (US Patent # 5,712,652) discloses a liquid crystal display device with AC generating circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Carter whose telephone number is 571-270-3006. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chris Kelley can be reached on 571-272-7331. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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